CLAIM AMENDMENTS:

The following listing replaces all previous listings of the claims:

1. (Currently amended) A semiconductor device, comprising:

a solid state device;

a semiconductor chip having a functional surface on which a functional element is formed, the semiconductor chip being bonded on a surface of the solid state device with the functional surface thereof facing the surface of the solid state device while maintaining a predetermined distance between the functional surface thereof and the surface of the solid state device;

a pillar-shaped connecting member configured to connect the functional surface of the semiconductor chip to the surface of the solid state device, a width of the pillar-shaped connecting member being constant;

an insulating film provided on the surface of the solid state device facing the semiconductor chip, the insulating film having an opening greater in size than the semiconductor chip when the surface of the solid state device facing the semiconductor chip is viewed from vertically above; and

a sealing layer that seals a space between the solid state device and the semiconductor chip,

wherein a difference in level caused by the opening is not located in a gap between the solid state device and the semiconductor chip.

2. (Previously presented) The semiconductor device according to Claim 1, wherein the sealing layer is provided in such a manner as to fill the opening with the sealing layer.

3. (Cancelled).

4. (Previously presented) The semiconductor device according to Claim 1, wherein the pillar-shaped connecting member is formed by bonding a connection pad provided on the solid state device and a projection electrode provided on the semiconductor chip.

5. (Cancelled).

6. (Previously presented) The semiconductor device according to Claim 1, wherein a distance between an outer periphery of the semiconductor chip and an edge of the opening of the insulating film is 0.1 mm or more when the surface of the solid state device facing the semiconductor chip is viewed from vertically above.

7. (Previously presented) The semiconductor device according to Claim 1, wherein the semiconductor chip is connected in a flip chip manner.

8. (New) The semiconductor device according to Claim 1, wherein the sealing layer covers the semiconductor chip up to a lower level than an upper end of a side surface of the semiconductor chip. (See Fig. 2D.)

9. (New) The semiconductor device according to Claim 1, wherein the solid state device is a wiring board formed by being wired on an insulating substrate. (See paragraph [0013] in the English specification.)

10. (New) The semiconductor device according to Claim 1, wherein the solid state device is a semiconductor substrate. (See paragraph [0013] in the English specification.)

11. (New) The semiconductor device according to Claim 1, wherein the insulating film is a solder resist. (See paragraph [0014].)

12. (New) The semiconductor device according to Claim 9, wherein a connection pad is formed on a surface of the wiring board, the surface of the wiring board opposing to the semiconductor chip. (See paragraph [0018] in the English specification.)

13. (New) The semiconductor device according to Claim 12, wherein the connection pad has a rectangular shape. (See paragraph 10018] in the English specification.)

14. (New) The semiconductor device according to Claim 11, wherein the solder resist has a thickness smaller than an interval between the semiconductor chip and a surface of the solid state device opposing thereto, the solid state device being a wiring board. (See paragraph [0019] in the English specification.)

15. (New) The semiconductor device according to Claim 9, wherein an electrode is formed at an end of the wiring board. (See paragraph [0031] in the English specification.)